Customer No.: 31561
Docket No.: 09946-US-PA-1
Application No.: 10/711,004

REMARKS

Present Status of the Application

Claims 1-10 remain pending of which claims 1 and 3 have been amended and claims 6-10 have been newly added, and claim 5 has been canceled without prejudice or disclaimer, to more explicitly describe the claimed invention. It is believed that no new matter adds by way of amendment to claims or otherwise to the application.

In the outstanding Office Action, claim 5 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; claims 1-2 and 4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoji et al. (US-5,349,221, hereinafter Shimoji) in view Shanware et al. "Reliability evaluation of HfSiON gate dielectric film with 12.8 a SiO2 equivalent thickness; claims 1-4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US-6,468,865, hereinafter Yang) in view of Shanware et al.; and claims 1-5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Kang et al. "Improved Thermal stability and device performance of ultra-thi (EOT<10A) gate dielectric MOSFET by using hafnium oxynitride (HfOxNy).

For at least the following reasons, Applicant respectfully submits that claims 1-4 and 6-10 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 112

The Office Action rejected to claim 5 under 35 U.S.C. 112, second paragraph, for failing to comply with enablement requirement.

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In response thereto, Applicants would like to thank the Examiner for pointing out the informality and accordingly canceled claim 5 without prejudice or disclaimer. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 103

I. The Office Action rejected claims 1-2 and 4 under 35 U.S.C. 103(a) as being unpatentable over Shimoji et al. (US-5,349,221, hereinafter Shimoji) in view Shanware et al. "Reliability evaluation of HfSiON gate dielectric film with 12.8 a SiO2 equivalent thickness.

In rejecting the above claims, the Office Action stated that Shimoji discloses every features of the claimed invention except for a tunneling dielectric layer comprised of HfSiON. However, the Office Action pointed out that Shanware suggests replacing the conventional silicon oxide by HfSiON in order to reduce gate-leakage and improve reliability. Therefore, it would have been obvious to a person skilled in the art at the time of the invention to modify Shimoji by including the HfSiON instead of silicon oxide in order to reduce gate-leakage and improve reliability of the device.

Applicants respectfully disagree and traverse the above rejections as set forth below.

The present invention is directed to a Read-Only Memory Device including a high-K tunneling dielectric layer. The proposed independent claim 1, among other things, recites at least [*a tunneling dielectric layer, disposed over the substrate, wherein the tunneling dielectric layer is formed with a material selected from the group consisting of*

HfSiON and HfO_xN_y, wherein the tunneling dielectric layer reduces leakage of electrons stored in the charge trapping layer into the substrate; an electron trapping layer, over the tunneling dielectric layer; a top dielectric layer, over the electron trapping layer; and a conductive layer, over the top dielectric layer]. The advantage of disposing the HfSiON or HfO_xN_y tunneling dielectric layer between the substrate and the electron trapping layer is that at least leakage of electrons stored in the charge trapping layer into the substrate can be effectively reduced.

Applicants respectfully submit that the present inventors have discovered that in the MEMORY DEVICE, when the thickness of the OXIDE tunneling layer is decreased beyond a critical thickness, the oxide tunneling layer may loose the capability to retard the electrons and therefore the electrons stored in the electron trapping layer may penetrate into substrate through the oxide tunneling layer. Thus, the stored information in the memory cell may be lost. In order to remedy this problem, the present inventors propose replacing the oxide tunneling layer with the HfSiON or HfO_xN_y tunneling dielectric layer.

Applicants respectfully submit that Shimoji, at FIG. 1, col. 4, lines 36-59, discloses a substrate 11, an insulating layer 19 comprised of ONO film formed over the substrate 11 and a gate 20 formed on the insulating layer 19. Furthermore, Shanware substantially teaches using a gate dielectric layer comprised of HfSiON material for reducing gate leakage problems.

Applicants would like to point out that a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the

source of the problem is identified. Therefore, the question here is whether Shimoji and Shanware recognized the cause of the leakage of electrons stored in the electron trapping layer into the substrate.

Applicants respectfully submit that because Shimoji substantially teaches a charge trapping layer 19 comprised of ONO on the substrate 11 and a gate 20 on the charge trapping layer 19, and fails to even mention the leakage of electrons stored in the charge trapping layer 19, and since Shanware recognizes the problems of GATE-LEAKAGE and suggests using HfSiON dielectric layer to reduce the GATE-LEAKAGE, and therefore it is clear that both Shimoji and Shanware fail to recognize the problems of the leakage of electrons stored in the electron trapping layer into the substrate, which the present inventors propose to solve.

Furthermore, Applicants would like to point out that a person of ordinary skill in the art is also presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate. Accordingly, because Shimoji fails to even mention the leakage of electrons stored in the charge trapping layer 19 and Shanware recognizes the problems of GATE-LEAKAGE and suggests using HfSiON dielectric layer to reduce the GATE-LEAKAGE, and therefore, one skilled in the art AT BEST would modify the structure of Shimoji by replacing the top oxide layer 18 formed between the gate 20 and the charge trapping layer 17 with HfSiON dielectric layer in order to reduce GATE-LEAKAGE as taught by Shanware. In other words, both Shimoji and Shanware substantially fail to teach, suggest or hint a HfSiON or HfO_xN_y tunneling dielectric layer between the substrate and the electron trapping layer for reducing leakage

of the electrons stored in the electron trapping layer.

Therefore, Applicants respectfully submit that Shimoji and Shanware, neither alone nor in combination, could possibly render every features of the proposed independent claim 1 obvious in this regard.

Because the newly added proposed independent claim 6 also recite features that are similar to the amended proposed independent claim 1, therefore Applicants similarly submit that claim 6 also patently defines over Shimoji and Shanware for at least the same reasons discussed above.

Claims 2, 4 and 10, and 7-9, which directly or indirectly depend from independent Claims 1 and 6, respectively, are also patentable over Shimoji and Shanware at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-2, 4 and 6-10 patently define over Shimoji and Shanware. Reconsideration and withdrawal of above rejections is respectfully requested.

2. The Office Action rejected claims 1-4 under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US-6,468,865, hereinafter Yang) in view of Shanware et al.

In rejecting the above claims, the Office Action stated that Yang discloses every features of the claimed invention except for a tunneling dielectric layer comprised of HfSiON. However, the Office Action pointed out that Shanware suggests replacing the conventional silicon oxide by HfSiON in order to reduce gate-leakage and improve reliability. Therefore, it would have been obvious to a person skilled in the art at the

time of the invention to modify Yang by including the HfSiON instead of silicon oxide in order to reduce gate-leakage and improve reliability of the device.

Applicants respectfully disagree and similarly (as discussed above) submit that because Yang, at FIGs. 7-8 and FIGs. 14-15, line 35 of col. 5 to line 6 of col. 10, discloses a SONOS comprising a substrate 10, a charge trapping layer 14 [14a (Oxide), 14b (Nitride) and 14c (Oxide)] over core region of the substrate 10 and a Gate Dielectric layer 22 or 23 over the peripheral region of the substrate 10 and polysilicon gates 28 formed over the top oxide layer 14c of the charge trapping layer 14 and the gate dielectric layer 23 respectively, and fails to even mention the leakage of electrons stored in the charge trapping layer, and since Shanware substantially teaches using a gate dielectric layer comprised of HfSiON material for reducing gate leakage problems, and therefore it is clear that both Shimoji and Shanware fail to recognize the problems of the leakage of electrons stored in the electron trapping layer into the substrate, which the present inventors propose to solve.

Applicants would like to point out that because Yang fails to even mention the leakage of electrons stored in the charge trapping layer and Shanware substantially teaches replacing the silicon oxide with HfSiON dielectric layer to reduce the gate leakage problems, and therefore Shanware AT BEST suggests one skilled in the art to replace the top oxide layer 14c and gate dielectric layer 23 with HfSiON dielectric layer of Yang. In other words, both Yang and Shanware substantially fail to teach, suggest or hint a HfSiON or HfO_xN_y tunneling dielectric layer between the substrate and the electron

trapping layer for reducing leakage of the electrons stored in the electron trapping layer. Accordingly, Applicants respectfully submit that Yang and Shanware, neither alone nor in combination, could possibly render every features of the proposed independent claim 1 obvious in this regard.

Because the newly added proposed independent claim 6 also recite features that are similar to the amended proposed independent claim 1, therefore Applicants similarly submit that claim 6 also patently defines over Yang and Shanware for at least the same reasons discussed above.

Claims 2-4, and 7-8, which directly or indirectly depend from independent Claims 1 and 6, respectively, are also patentable over Yang and Shanware at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-4 and 6-8 patently define over Yang and Shanware. Reconsideration and withdrawal of above rejections is respectfully requested.

3. *The Office Action rejected claims 1-5 under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Kang et al. "Improved Thermal stability and device performance of ultra-thi (EOT<10A) gate dielectric MOSFET by using hafnium oxynitride (HfOxNy).*

In rejecting the above claims, the Office Action stated that Yang discloses every features of the claimed invention except for a tunneling dielectric layer comprised of HfSiON. However, the Office Action pointed out that Kang suggests improving thermal

stability and device performance by using HfSiON as gate dielectric material. Therefore, it would have been obvious to a person skilled in the art at the time of the invention to modify Yang by including the HfSiON suggested by Kang to improve the thermal stability and device performance.

Applicants respectfully disagree and traverse the above rejections as follows. As discussed above, Yang, at FIGs. 7-8 and FIGs. 14-15, line 35 of col. 5 to line 6 of col. 10, discloses a SONOS comprising a substrate 10, a charge trapping layer 14 [14a (Oxide), 14b (Nitride) and 14c (Oxide)] over core region of the substrate 10 and a Gate Dielectric layer 22 or 23 over the peripheral region of the substrate 10 and polysilicon gates 28 formed over the top oxide layer 14c of the charge trapping layer 14 and the gate dielectric layer 23 respectively. Furthermore, Kang substantially teaches using a GATE Dielectric layer comprised of HfSiON material for improving the thermal stability and device performance.

Applicants would like to point out that because Yang substantially fails to even mention the leakage of electrons stored in the charge trapping layer and Kang substantially teaches replacing the silicon oxide GATE DIELECTRIC layer with HfSiON dielectric layer to improve the thermal stability, and therefore Kang AT BEST suggests one skilled in the art to replace the top oxide layer 14c and gate dielectric layer 23 with HfSiON dielectric layer of Yang. In other words, both Yang and Kang substantially fail to teach, suggest or hint a HfSiON or HfO_xN_y tunneling dielectric layer between the substrate and the electron trapping layer for reducing leakage of the electrons stored in the electron trapping layer. Accordingly, Applicants respectfully submit that Yang and Kang,

neither alone nor in combination, could possibly render every features of the amended proposed independent claim 1 in this regard.

Because the newly added proposed independent claim 6 also recite features that are similar to the amended proposed independent claim 1, therefore Applicants similarly submit that claim 6 also patently defines over Yang and Kang for at least the same reasons discussed above.

Claims 2-4 and 10, and 7-9, which directly or indirectly depend from independent Claims 1 and 6, respectively, are also patentable over Yang and Kang at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-4 and 6-10 patently define over Yang and Kang. Reconsideration and withdrawal of above rejections is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-4 and 6-10 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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